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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,008	11/18/2003	Lakshman Ramakrishnan	15030US02	4199
23446 7590 03/01/2010 MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661				
EXAMINER				
SENFL BEHROOZ M				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/716,008

Applicant(s)

RAMAKRISHNAN ET AL.

Examiner

BEHROOZ SENFI

Art Unit

2621

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,5,7 and 9-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10 and 11 is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/2/2009 has been entered.

Claim Objections

2. Claim 1 objected to because of the following:

It is noted that, the wording "2x2 pixels block" as newly added into claim 1, fails to comply with the written description requirement. However examiner notice that the "8x8 and/or 16x16" pixels block as specifies in the disclosure of the invention would encompasses "2x2 pixels" block.

Response to Amendment

3. Applicant's arguments filed 10/2/2009 have been fully considered but they are not persuasive.

Response to remarks:

Applicant asserts (remarks; page 10, lines 1-4) that the reference "Inoue" does not teach storing/writing data continuously in the memory.

Examiner respectfully disagrees; applicant should note that, Inoue in (col. 10, lines 61-col. 11, lines 10) teaches storing/writing data continuously in the memory

channels. Therefore the claims are finally rejected for the same reason as set forth in the last Office Action, mailed 6/2/2009. The rejections are being restated for applicant convenience.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 7,079,583) in view of Inoue (US 5,920,352) Uchida (US 5,461,486).

Regarding claim 1, Yoshioka '583 discloses, a method for storing macro-blocks In a memory (i.e., fig. 3, memory 3 is used for storing macro-blocks), the method comprising; decoding a macro-block, thereby resulting in a decoded macro-block, the decoded macro-block comprising pixels (i.e., fig. 3, decoder 1002 including routine processing 1004 used for decoding a macro-block, see col. 11, lines 21 – 44 and col. 16, lines 12 – 13); and executing an instruction, wherein the instruction causes writing the decoded macro-block to the memory (i.e., fig. 3, illustrates decoder unit 1002 including, routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-block and stores, e.g., writes the decoded block/macro-block to the memory unit 3, see col. 11, lines 39 – 50), outputting

a frame comprising the decoded macro-block to a display device (i.e., col. 3, lines 54-56 and col. 10, lines 53-57).

Although, Yoshioka '583 show writing decoded macro-block composed of writing decoded luminance matrix blocks (Y) and decoded chrominance matrix blocks (Cb) and (Cr) to the memory, and wherein the block comprises at least 2x2 pixels block (i.e., col. 9, lines 36-41 and col. 11, lines 30-35, thus encompasses 2x2 pixels block).

Yoshioka '583 is silent in regards to explicit of arrangement for continuously writing the decoded block in the, "first portion of the memory; second portion of the memory; third portion of the memory; and the first portion, second portion, and third portion being contiguous".

Inoue teaches the above-mentioned claimed limitations are well known in the art. In particular, Inoue teaches the arrangement of continuous writing a block of decoded luminance to a first portion of the memory (i.e., as shown in figs. 1C, luminance matrix/block Y are stored in the respective memory areas assigned to, e.g., first portion of memory, col. 11, lines 1-9 and 39-47), writing a first matrix/block of decoded chrominance to second portion of the memory (i.e., as shown in figs. 1C, decoded chrominance block/matrix Cb are stored in the respective memory areas assigned to, e.g., second portion of memory, col. 11, lines 1-9 and 39-47), writing a matrix/block of decoded second chrominance to a third portion of the memory (i.e., as shown in figs. 1C, decoded second chrominance block Cr are stored in the respective memory areas assigned to, e.g., second portion of memory, col. 11, lines 1-9 and 39-47), and the first portion, second portion, and third portion being contiguous (i.e., as shown in fig. 1C, the

first portion (Y), second portion (Cb) and third portion (Cr) of the memory are being contiguous, col. 11, lines 39-47 and col. 14, lines 35-41), also teaches wherein the block comprises at least 2x2 pixels block (i.e., col. 2, lines 23-27, 59-60 and col. 6, lines 48-51, thus encompasses 2x2 pixels block).

In view of the above, having the digital signal processing of Yoshioka showing writing decoded macro-block composed of luminance blocks (Y) and chrominance blocks (Cb) and (Cr) to the memory, and given the well-established teaching of Inoue where the luminance matrix is written in a first portion of the memory; and first chrominance matrix to second portion of the memory and a second chrominance matrix to a third portion of the memory, where the first portion, second portion, and third portion being contiguous, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Inoue, since Inoue suggest in col. 14, lines 44-46 that such a modification would allow data representing image fields to be stored and fetched in several different ways.

Regarding claim 5, the limitations claimed are substantially similar to claim 1 above, and is the circuit of the method of claim 1 for string macro-blocks in a memory, therefore the ground for rejecting the method of claim 1 also applies to the circuit claim, and as for the additional limitation, a computer readable medium storing an executable instruction (i.e., figs. 3 - 4, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 - 67 and col. 11, lines 39 - 50, also Inoue,

fig. 2D-3A), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50, also Inoue, fig. 2D-3A).

Regarding claim 9, the combination of Yoshioka and Inoue teaches, wherein one portion of a single data word is part of the second portion of the memory where the first matrix of chrominance pixels are written and another portion of the single data word is part of the third portion of the memory where the second matrix of chrominance pixels are written (i.e., figs. 2C and 3Acol. 4, lines 44-47 of Inoue).

6. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 7,079,583) in view of Uchida (US 5,461,486) and Inoue (US 5,920,352).

Regarding claim 3, the limitations claimed have been analyzed and rejected with respect to claim 1 above. As for, executing an instruction, wherein the instruction causes writing the macro-blocks to the memory (Yoshioka; fig. 3, describes routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-blocks and stores/writes the decoded macro-block to the memory unit 3, see col. 11, lines 39 – 50), outputting a frame comprising the decoded macro-block to a display device (Yoshioka; col. 3, lines 54-56 and col. 10, lines 53-57). Furthermore;

The combination of Yoshioka and Inoue teaches the arrangement of continuously writing blocks of decoded macro-blocks, luminance and chrominance pixels in the

memory; but is silent in regards to explicitly look at five macro-blocks, five luminance and five chrominance pixels.

However, Uchida teaches, compression and decompression, e.g., reproduction, operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas (i.e., col. 7, lines 4 – 41, col. 15, lines 20 – 21).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the image memory storage of Inoue by writing the length of five macro-blocks, including five decoded luminance and five decoded chrominance pixels, thus such modification would improved image quality in the high speed reproduction of the digital video signal, as suggested by Uchida (col. 2, lines 57 – 58).

Regarding claim 7, the limitations claimed are substantially similar to claim 3 above, and is the circuit of the method of claim 3 for string macro-blocks in a memory, therefore the ground for rejecting the method of claim 3 also applies to the circuit claim, and as for the additional limitation, a computer readable medium storing an executable instruction (figs. 3 – 4 of Yoshioka, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 – 67 and col. 11, lines 39 - 50), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3 of Yoshioka, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50).

Allowable Subject Matter

7. Claims 10-11 are allowed.
8. The following is an examiner's statement of reasons for allowance: The prior art of the record fails to anticipate or fairly suggest the arrangement for storing macro-blocks in a memory, as specifies in claims 10 and 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Behrooz Senfi whose telephone number is 571-272-7339. The examiner can normally be reached on M-F 7:00-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Behrooz Senfi/
Primary Examiner
Art Unit 2621